UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/785,181	02/25/2004	Nobuyuki Endo	OKI 412	3382

7590 06/27/2006

RABIN & BERDO, P.C.
Suite 500
1101 14th Street
Washington, DC 20005

EXAMINER	
AMAYA, CARLOS DAVID	
ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 06/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/785,181	ENDO, NOBUYUKI	
	Examiner	Art Unit	
	Carlos Amaya	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02/25/2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/5/06,2/25/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 5 is objected to because of the following informalities: In Claim 5, line 3 it appears that "and" should be replaced by "or". For the purpose of applying art to the claim, In Claim 5 examiner replaced "and" for "or". Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

3. Claims 1-5 are rejected under 35 U.S.C. 102(b) as being anticipated by Bennett (US 6,288,613).

With respect to claim 1 Bennett discloses a semiconductor integrated circuit device comprising: a power wiring whose one end is connected to a power supply (Power wiring consist of the wire extending from FET 20); a ground wiring (Line 22) whose one end is connected to a ground (Line 22 is connected to 0V or ground); and a plurality of circuits connected in parallel between the power wiring and the ground wiring (Column 4 lines 62-65), wherein the other end of the ground wiring is connected to a current generating section (Bias circuit 26 Figure 2) for generating a predetermined current (Column 3 lines 19-23, Column 3 lines 29-30) in a state in which the section is

connected to a negative power supply (Bias circuit 26 is connected to line 38, which is connect to Negative voltage -V).

With respect to claim 2 Bennett discloses a semiconductor integrated circuit device comprising: a power wiring whose one end is connected to a power supply (Power wiring consist of the wire extending from FET 20); a ground wiring (Line 22) whose one end is connected to a ground (Line 22 is connected to 0V or ground); a plurality of circuits connected in parallel between the power wiring and the ground wiring (Column 4 lines 62-65); and a current generating section (Bias circuit 26) whose one end is connected to the other end of the ground wiring to generate a predetermined current (Column 3 lines 19-23, Column 3 lines 29-30) in a state in which the other end of the section is connected to a negative power supply (Negative voltage –V, Figure 2).

With respect to claim 3 Bennett discloses a semiconductor integrated circuit device comprising: a power wiring (Power wiring consist of the wire extending from FET 20) whose one end is connected to a power supply (Positive voltage V+); a ground wiring (Line 22) whose one end is connected to a ground (0V); a plurality of circuits connected in parallel between the power wiring and the ground wiring (Column 4 lines 62-65); a negative power supply (Negative voltage -V); and a current generating section (Bias circuit 26) whose one end is connected to the ground wiring and whose other end is connected to the negative power supply to generate a predetermined current (Bias circuit 26 is connected to ground line 22 and line 38, which is connect to Negative voltage –V to generate a predetermine voltage; Column 3 lines 19-23, Column 3 lines 29-30).

With respect to claim 4 Bennett discloses the semiconductor integrated circuit device according to claim 1, wherein the current generating section is disposed in a wiring portion most distant from a portion in which a ground potential is supplied to the ground wiring (As can be seen on figure 2 the bias circuit 26 is placed distant from the ground potential 0V that supplies the ground line 22).

With respect to claim 5 Bennett discloses the semiconductor integrated circuit device according to claim 1, wherein the current generating section is either one of a current source or an operating circuit which consumes a predetermined current to operate (Figure 2 shows FETs 28 and 30 of bias circuit 26, as it is well known in the art transistors behave depending on a current supply to its gate, thus they consume current to operate; accordingly figure 2 shows resistors 32 and 34).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bennett (US 6,288,613) in view of Wedding (US 2004/0008733).

With respect to claim 6 Bennett discloses the semiconductor integrated circuit device according to claim 5, however, Bennett does not disclose expressly that the

operating circuit that consumes the predetermined current to operate is a clock generator which outputs a clock signal.

Wedding discloses a clock generator circuit 7, Figure 3 that outputs a clock signal to phase shifters 9' and 9"; it is understood that in order to operate the clock generator must be supplied with a predetermined current to obtain a desired clock signal.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have added a clock generator to the bias circuit disclosed by Bennett.

The suggestion or motivation for doing so would have been to provide a more reliable means to operate the circuits, specifically gate operated devices that performed an operation in response to an input signal.

With respect to claim 7 Bennett discloses the semiconductor integrated circuit device according to claim 6, however, Bennett does not disclose expressly that the clock generator is connected to a level shifter for converting a level of the outputted clock signal to supply the clock signal to the plurality of circuits.

Wedding discloses a clock generator circuit 7, Figure 3, the clock generator outputs a clock signal to phase shifters 9' and 9" to supply plurality of circuits (Data sources 5' and 5"), Page 2, Column 2 Paragraph (0035) lines 10-12.

It would have been obvious to add the shifters disclosed by Wedding to the bias circuit disclosed by Bennett, for the purpose of supplying a predetermined signal to the circuits (Page 2, Column 2 Paragraph (0035) lines 2-28).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to the examiner's supervisor, Brian Sircus who can be reached on (571)272-2800. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

CA

CHAU N. NGUYEN
PRIMARY EXAMINER